PATENT APPLICATION TRANSMITTAL LETTER
(Large Entity)

Docket No.
D730

JC540 U.S. PTO 09/208325 12/09/98

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Jeffrey A. Shields & Kelwin Ko

For: **A SACRIFICIAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUHPUT**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EJ018612723US**
- ☒ **Seven (7)** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☐ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☒ Other: **Assignment**

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	5	- 20 =	0	x	$18.00	$0.00
Indep. Claims	1	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
					TOTAL FILING FEE	$760.00

- ☐ A check in the amount of to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **01-0365** as described below. A duplicate copy of this sheet is enclosed.
  - ☒ Charge the amount of **$760.00** as filing fee.
  - ☒ Credit any overpayment.
  - ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
  - ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: **12/9/98**

H. D. Nelson
Signature
H. Donald Nelson, Reg. No. 28,980

cc:

P01LARGE/REV06

A SACRIFICIAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT

Jeffrey A. Shields

Kelwin Ko

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to a method of manufacturing semiconductor devices and more specifically, this invention relates to a method of manufacturing semiconductor devices in which a layer of TiN formed on a surface of metal structures is removed after metal etch.

2. Discussion of the Related Art

In many of the current semiconductor manufacturing processes, the pad etch process consists of etching a layer of interlayer dielectric (ILD) and stopping on a layer of TiN on top of underlying metal structures. The layer of TiN is then etched completely down to the surface of the underlying metal structures. As is known in the semiconductor manufacturing art, pad etch is notoriously slow because of the substantial thickness of the final dielectric film and because of the requirement to completely remove the layer of TiN. The trend in the semiconductor manufacturing art is to make the layer of TiN sufficiently thick in order to prevent developer attack of the aluminum under TiN film, see the paper by E.G. Colgan, et al., "Formation Mechanism of Ring Defects during Metal RIE," 1994 VMIC Conference, June 7-8, 1994, page 284-286. Because it is necessary to completely remove the layer of TiN during pad etch so it will not interfere with the gold wire bonding process, the increased thickness of the layer of TiN increases the time required for pad etch.

Figures 1A – 1J show a prior art method of manufacturing a semiconductor device in which the layer of TiN formed on metal structures are etched during the pad etch process.

Figure 1A shows a partially completed semiconductor device **100**. The partially completed semiconductor device **100** includes a layer of material **102** that is typically a layer of an interlayer dielectric (ILD) formed from a material such as silicon dioxide. The layer **102** of interlayer dielectric is formed over the final metal layer **104**. The layer **104** is

a layer of metal that will be etched to form conductive interconnects from one portion of the semiconductor device **100** that will form pads that will be connected to external structures during the gold wire bonding process. The layer **104** is typically formed from aluminum. A layer **106** of TiN is formed on the surface of the layer **104**. The layer **106** of TiN serves as both a barrier layer and as an anti-reflective coating. A layer **108** of photoresist is formed on the surface of the layer **106** of TiN.

Figure 1B shows the partially completed semiconductor device **100** as shown in **Figure 1A** with the layer of photoresist **108** patterned and developed forming holes **110** and **112** in the layer **108** of photoresist that expose portions of the layer **106** of TiN.

Figure 1C shows the partially completed semiconductor device **100** as shown in **Figure 1B** after an etch process to etch the exposed portions of the layer **106** of TiN and exposing portions of the metal layer **104**.

Figure 1D shows the partially completed semiconductor device **100** as shown in **Figure 1C** after an etch process to etch the exposed portions of the metal layer **104** down to the surface of the layer **102** of interlayer dielectric.

Figure 1E shows the partially completed semiconductor device **100** as shown in **Figure 1D** with the layer of photoresist **108** removed.

Figure 1F shows the partially completed semiconductor device **100** as shown in **Figure 1E** with a blanket layer **114** of interlayer dielectric formed on the surface of the semiconductor device **100** and filling the holes **110** and **112**.

Figure 1G shows the partially completed semiconductor device **100** as shown in **Figure 1F** after a layer **116** of photoresist is formed on the surface of the layer **114** of interlayer dielectric. The layer **116** of photoresist is patterned and developed to form holes **118, 120,** and **122** that expose portions of the layer **114** of interlayer dielectric.

Figure 1H shows the partially completed semiconductor device **100** as shown in **Figure 1G** after an etch process to etch exposed portions of the layer **114** of interlayer dielectric exposing portions of the layer **106** of TiN.

Figure 1I shows the partially completed semiconductor device **100** as shown in **Figure 1H** after an etch process to etch the exposed portions of the layer **106** of TiN.

The step of completely etching the layer **106** of TiN during the pad etch process causes a slow down in the throughput of the semiconductor device during the manufacturing process.

Therefore, what is needed is a manufacturing process that does not require the step of etching the TiN layer during pad etch.

SUMMARY OF THE INVENTION

According to the present invention, the foregoing and other objects and advantages are obtained by a method of manufacturing semiconductor devices wherein a layer of TiN overlying metal structures in the final metal layer is removed after final metal etch. In accordance with one aspect of the invention, the method involves forming a final layer of metal on a layer of interlayer dielectric, forming a layer of TiN on the final layer of metal, forming a layer of photoresist on the layer of TiN, patterning and developing the layer of photoresist exposing portions of the final metal layer, and etching the exposed portions of the final metal layer forming metal structures. The layer of photoresist and layer of TiN are removed.

In another aspect of the invention, a blanket layer of interlayer dielectric is formed on the surface of the semiconductor device after the layer of photoresist and layer of TiN are removed. A second layer of photoresist is patterned and developed exposing portions of the interlayer dielectric overlying the metal structures. The exposed portions of the interlayer dielectric are etched down to the surface of the metal structures.

In still another aspect of the invention, the layer of photoresist and the layer TiN are removed by a process utilizing fluorine containing gas chemistry at an elevated temperature.

The described method of manufacturing semiconductor devices thus provides a method of removing the layer of TiN formed on the final metal layer structures resulting in improved throughput during pad etch.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become readily apparent to those skilled in the art from the following description, there is shown and described an embodiment of this invention simply by way of illustration of the best mode to carry out the invention. As will be realized, the invention is capable of other embodiments and its several details are capable of modifications in various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings and detailed description will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and

further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figures 1A – 1J show a prior art method of manufacturing a semiconductor device in which a layer of TiN formed on a metal structure is etched during the pad etch process, wherein;

Figure 1A shows a partially completed semiconductor device showing the final metal layer with a layer of TiN formed on the metal layer and a layer of photoresist formed on the layer of TiN;

Figure 1B shows the partially completed semiconductor device as shown in **Figure 1A** with the layer of photoresist patterned and developed forming holes in the photoresist exposing portions of the layer of TiN;

Figure 1C shows the partially completed semiconductor device as shown in **Figure 1B** after an etch process etches the exposed portions of the layer of TiN exposing portions of the metal layer;

Figure 1D shows the partially completed semiconductor device as shown in **Figure 1C** after an etch process etches the exposed portions of the metal layer exposing portions of a layer of interlayer dielectric underlying the metal layer;

Figure 1E shows the partially completed semiconductor device as shown in **Figure 1D** with the layer of photoresist removed;

Figure 1F shows the partially completed semiconductor device as shown in **Figure 1E** with a blanket layer of interlayer dielectric formed on the surface of the semiconductor device;

Figure 1G shows the partially completed semiconductor device as shown in **Figure 1F** after a layer of photoresist has been formed on the surface of the layer of interlayer dielectric and after the layer of photoresist has been patterned and developed exposing selected portions of the layer of interlayer dielectric;

Figure 1H shows the partially completed semiconductor device as shown in **Figure 1G** after an etch process to etch the exposed portions of the layer of interlayer dielectric down to the layer of TiN;

Figure 1I shows the partially completed semiconductor device as shown in **Figure 1H** after an etch process to etch the exposed layer of TiN;

Figures 2A – 2G show a method of manufacturing a semiconductor device in accordance with the present invention; wherein;

Figure 2A shows the partially completed semiconductor device as shown in **Figure 1D** after the layer of photoresist has been removed;

Figure 2B shows the partially completed semiconductor device as shown in **Figure 2A** after the layer of TiN has been removed from the surfaces of metal structures formed in previous processing steps;

Figure 2C shows the partially completed semiconductor device as shown in **Figure 2B** with a blanket layer of interlayer dielectric formed on the surface of the semiconductor device;

Figure 2D shows the partially completed semiconductor device as shown in **Figure 2C** after a layer of photoresist has been formed on the surface of the layer of interlayer dielectric and after the layer of photoresist has been patterned and developed exposing selected portions of the layer of interlayer dielectric;

Figure 2E shows the partially completed semiconductor device as shown in **Figure 2D** after an etch process to etch the exposing portions of the layer of interlayer dielectric; and

Figure 2F shows the partially completed semiconductor device as shown in **Figure 2E** after the layer of photoresist has been removed.

DETAILED DESCRIPTION

Reference is now made in detail to specific embodiments of the present invention which illustrate the best mode presently contemplated by the inventors for practicing the invention.

Figures 2A –2G show a method manufacturing a semiconductor device in accordance with the present invention.

Figure 2A shows the partially completed semiconductor device **100** as shown in **Figure 1D** with the layer **108** of photoresist removed.

Figure 2B shows the partially completed semiconductor device **100** as shown in **Figure 2A** with the layer **106** of TiN removed. The layer **108** of photoresist and the layer **106** of TiN are stripped during the same process step. One such method is to use a fluorine containing gas chemistry at elevated temperatures. For example, it has been shown that TiN and the resist can be removed effectively using a CF_4/O_2 gas chemistry at elevated temperatures. Typical applied power is in a range of 500 to 1000W at a pressure in a range of 500 to 2000mTorr. Typical gas flow rates are in the range of 100 to 500 sccm. The TiN removal rate is strongly dependent on the wafer temperature and CF_4 gas

flow, with higher removal rates at higher temperature and higher flow rates. TiN removal rates in excess of 2000Å/minute were achieved at 120°C wafer temperature, with substantially higher removal rates as temperatures were increased up to 240°C. This has been demonstrated in both an inductively-coupled resist stripper and a downstream microwave resist stripper.

Figure 2C shows the partially completed semiconductor device **100** as shown in **Figure 2B** with a blanket layer **114** of interlayer dielectric formed on the surface of the semiconductor device **100** and filling the holes **110** and **112**.

Figure 2D shows the partially completed semiconductor device **100** as shown in **Figure 2C** after a layer **116** of photoresist is formed on the surface of the layer **114** of interlayer dielectric. The layer **116** of photoresist is patterned and developed to form holes **118, 120**, and **122** that expose portions of the layer **114** of interlayer dielectric.

Figure 2E shows the partially completed semiconductor device **100** as shown in **Figure 2C** after an etch process to etch exposed portions of the layer **114** exposing portions of the layer **104**.

Figure 2F shows the partially completed semiconductor device **100** as shown in **Figure 2E** with the layer **116** of photoresist removed.

In summary, the results and advantages of the method of the present invention can now be fully realized. The method of removing the layer of TiN after final metal etch thus provides increased throughput during pad etch.

The foregoing description of the embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device, wherein the method comprises:

forming a final layer of metal on a layer of interlayer dielectric in the semiconductor device;

forming a layer of TiN on the final layer of metal;

forming a first layer of photoresist on the layer of TiN;

patterning and developing the first layer of photoresist exposing portions of the layer of TiN;

etching holes in the layer of TiN and the final layer of metal exposing portions of the interlayer dielectric, wherein metal structures are formed; and

removing the first layer of photoresist and the layer of TiN.

2. The method of Claim 1 further comprising forming a blanket layer of interlayer dielectric on the surface of the semiconductor device.

3. The method of Claim 2 further comprising:

forming a second layer of photoresist on the blanket layer of interlayer dielectric; and

patterning and developing the second layer of photoresist exposing portions of the blanket layer of interlayer dielectric overlying metal structures; and

etching the exposed portions of the blanket layer of interlayer dielectric down to the metal structures.

4. The method of Claim 3 further comprising removing the second layer of photoresist.

5. The method of Claim 1 wherein the first layer of photoresist and the layer of TiN is etched by a process utilizing fluorine containing gas chemistry at an elevated temperature.

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Kelwin Ko

ABSTRACT

A method of manufacturing a semiconductor device wherein a final layer of metal is formed on a layer of interlayer dielectric, forming a layer of TiN on the final layer of metal, forming a layer of photoresist on the layer of TiN, patterning and developing the layer of photoresist exposing portions of the final metal layer, and etching the exposed portions of the final metal layer forming metal structures. The layer of photoresist and layer of TiN are removed. A blanket layer of interlayer dielectric is formed on the surface of the semiconductor device. A second layer of photoresist is formed on the blanket layer of interlayer dielectric. The second layer of photoresist is patterned and developed exposing portions of the interlayer dielectric overlying the metal structures. The exposed portions of the interlayer dielectric are etched down to the surface of the metal structures.

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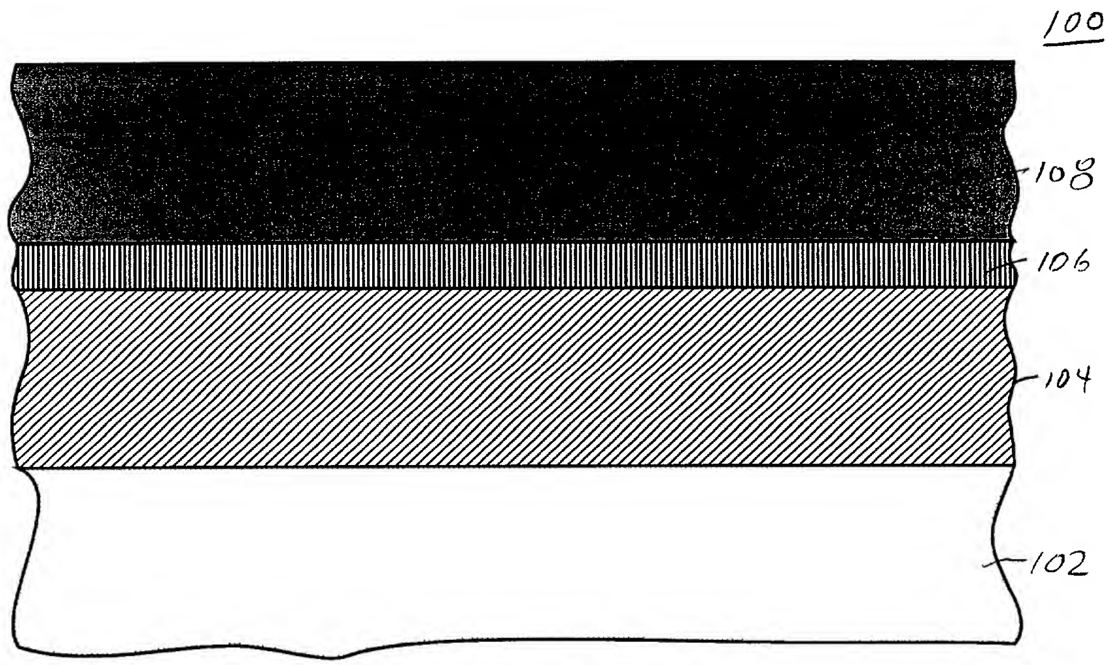

FIGURE 1A (PRIOR ART)

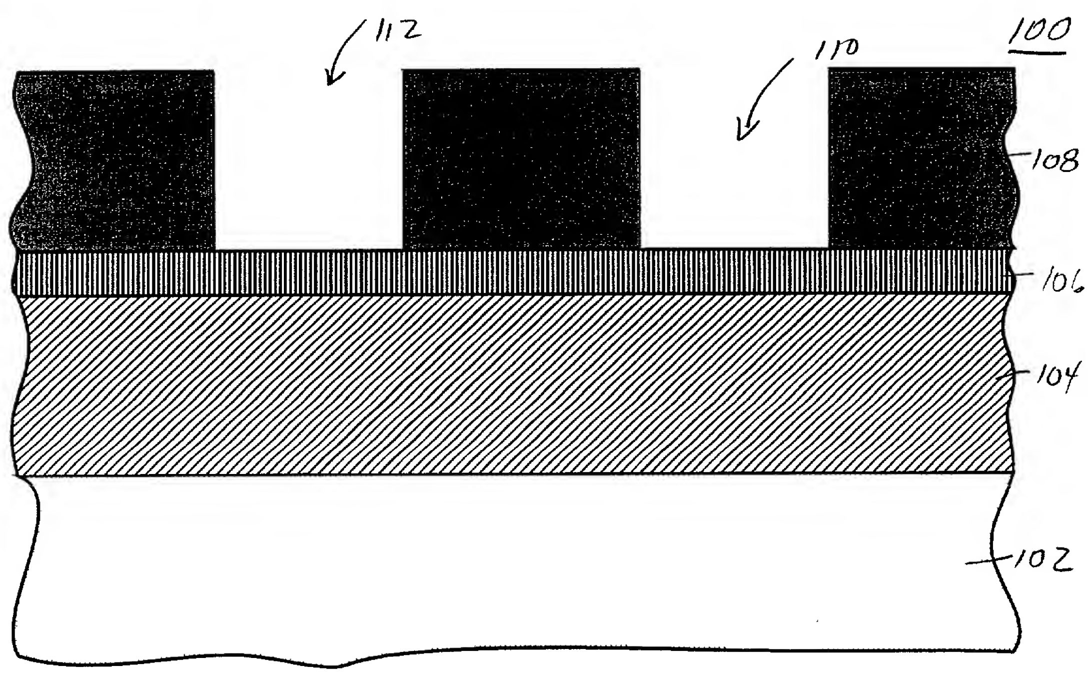

FIGURE 1B (PRIOR ART)

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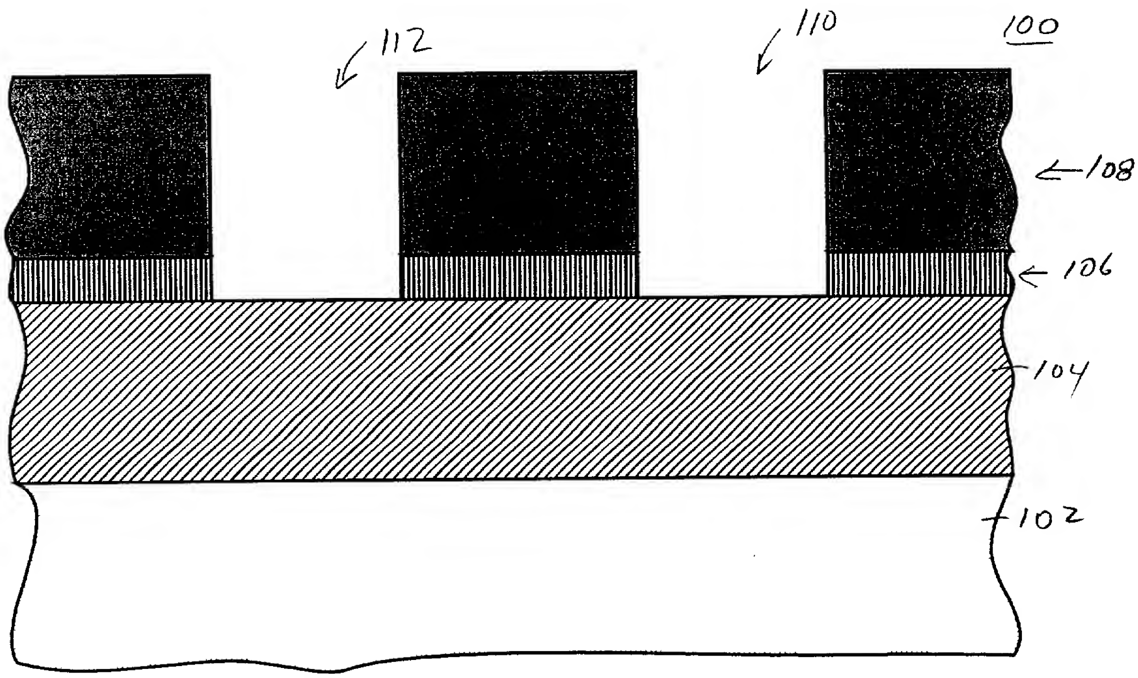

FIGURE 1C (PRIOR ART)

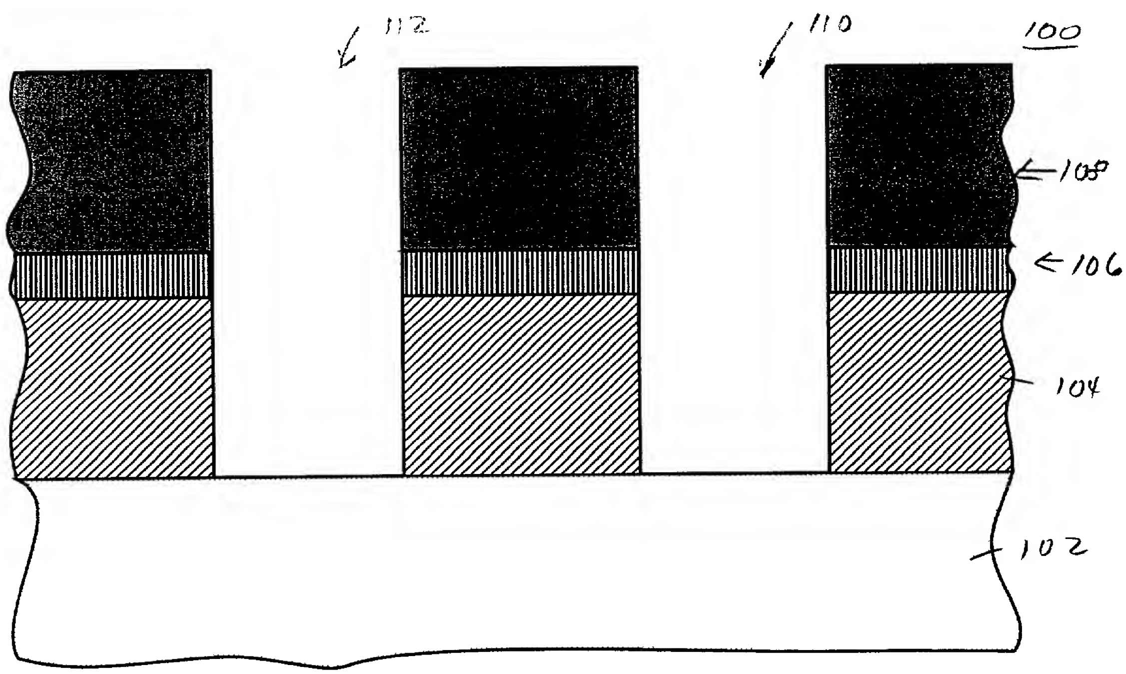

FIGURE 1D (PRIOR ART)

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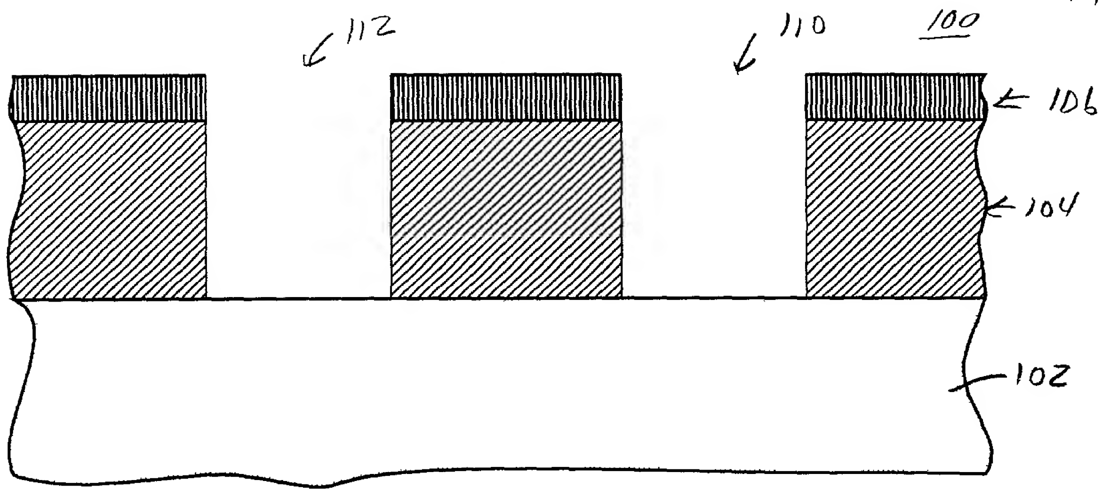

FIGURE 1E (PRIOR ART)

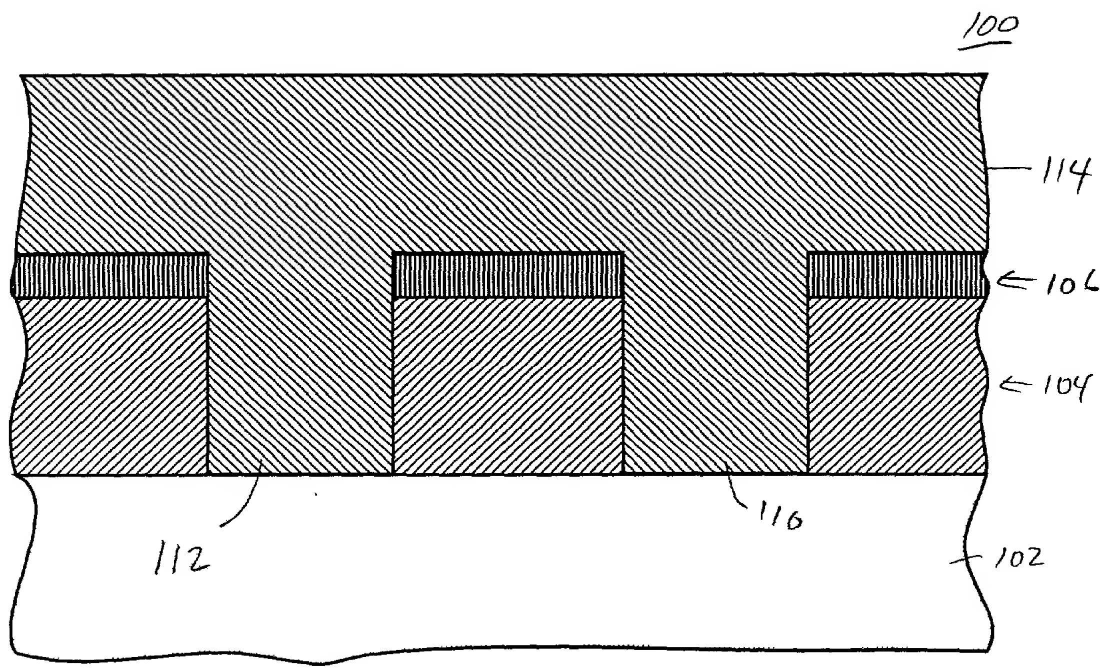

FIGURE 1F (PRIOR ART)

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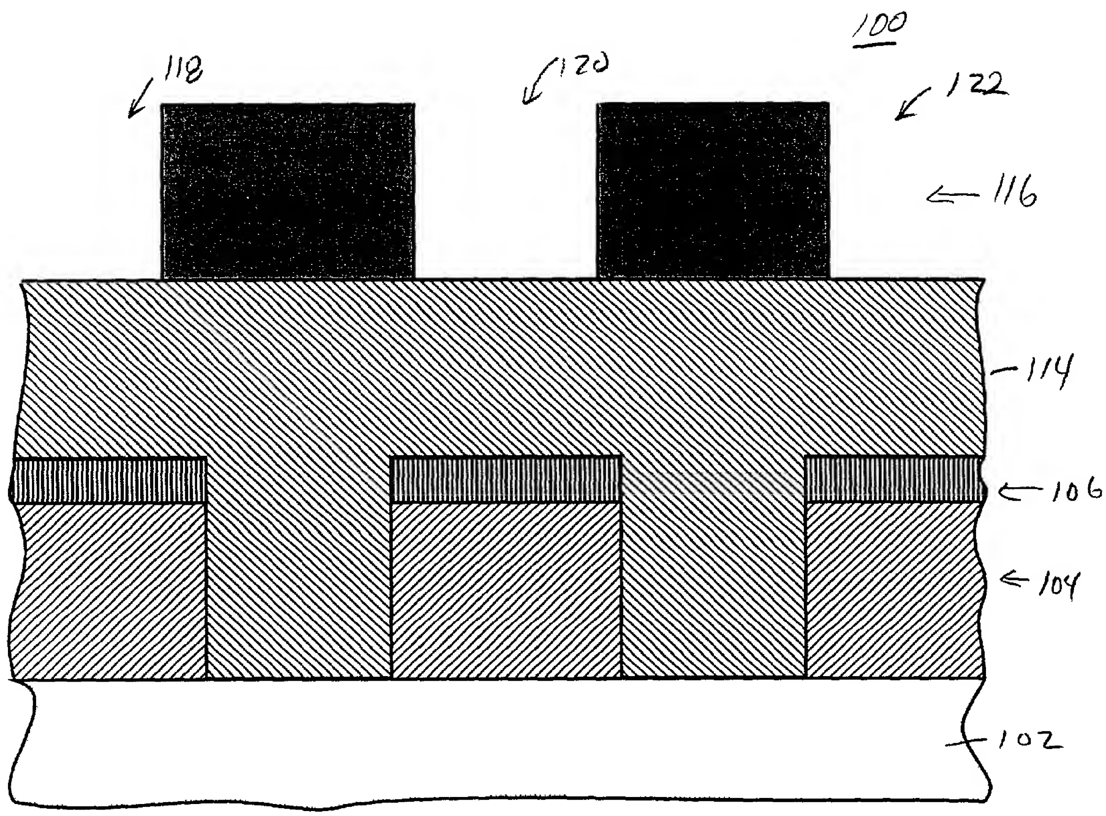

FIGURE 1G (PRIOR ART)

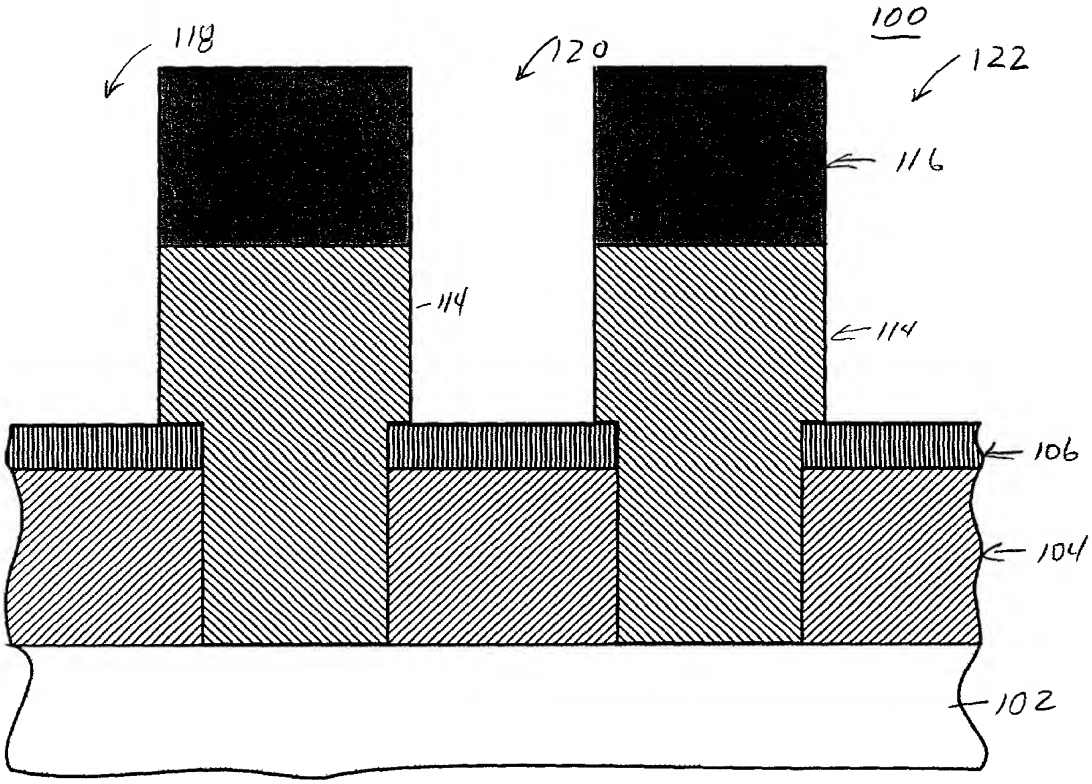

FIGURE 1H (PRIOR ART)

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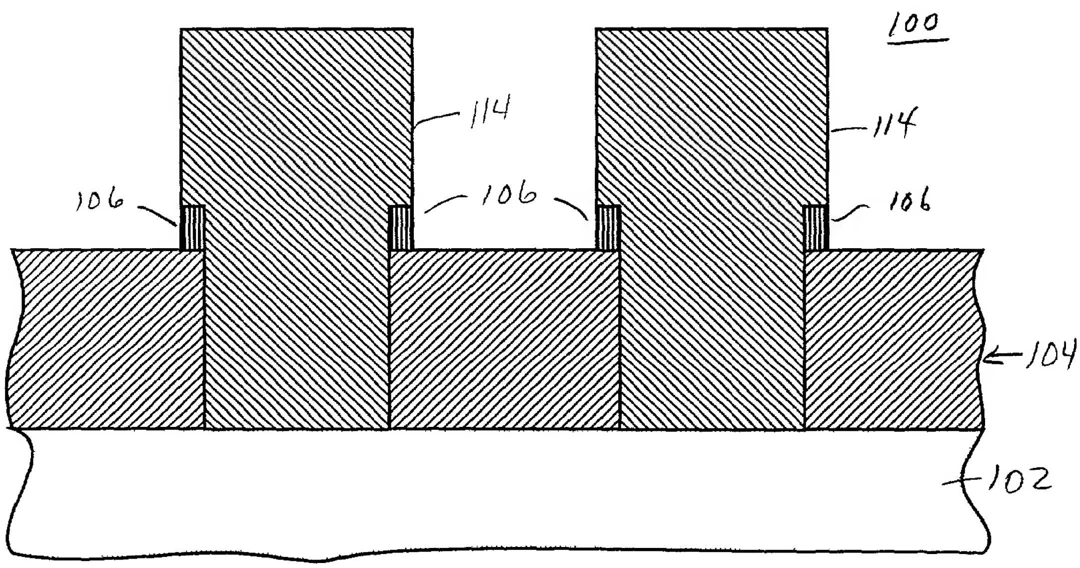

FIGURE 1I (PRIOR ART)

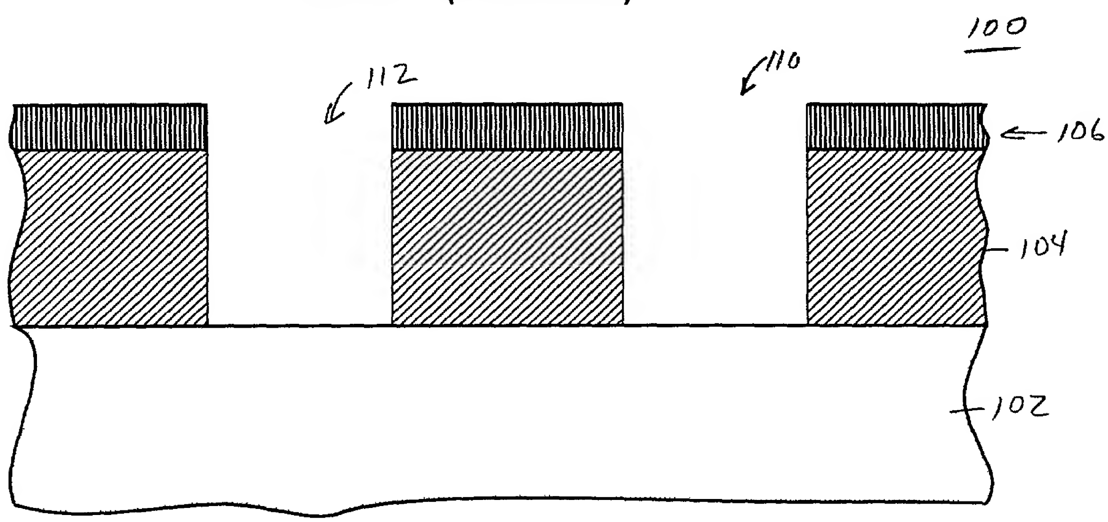

FIGURE 2A

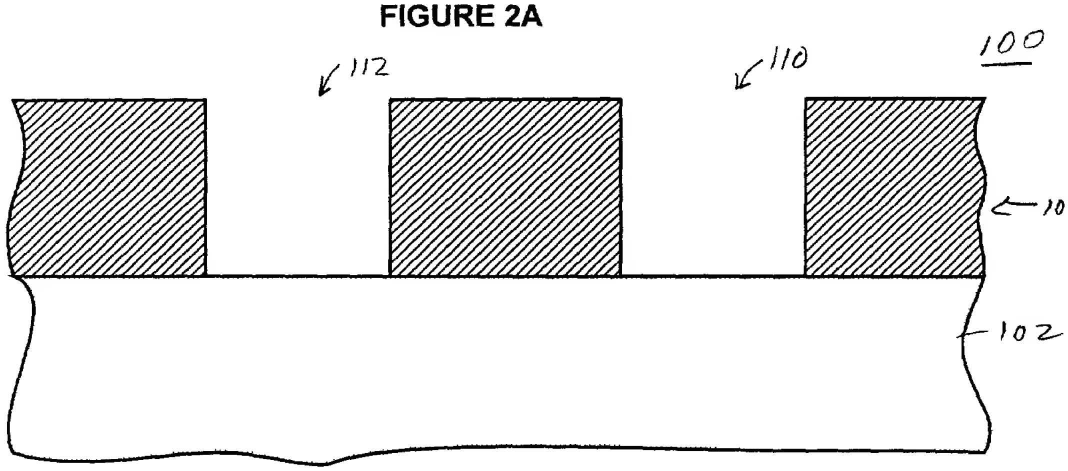

FIGURE 2B

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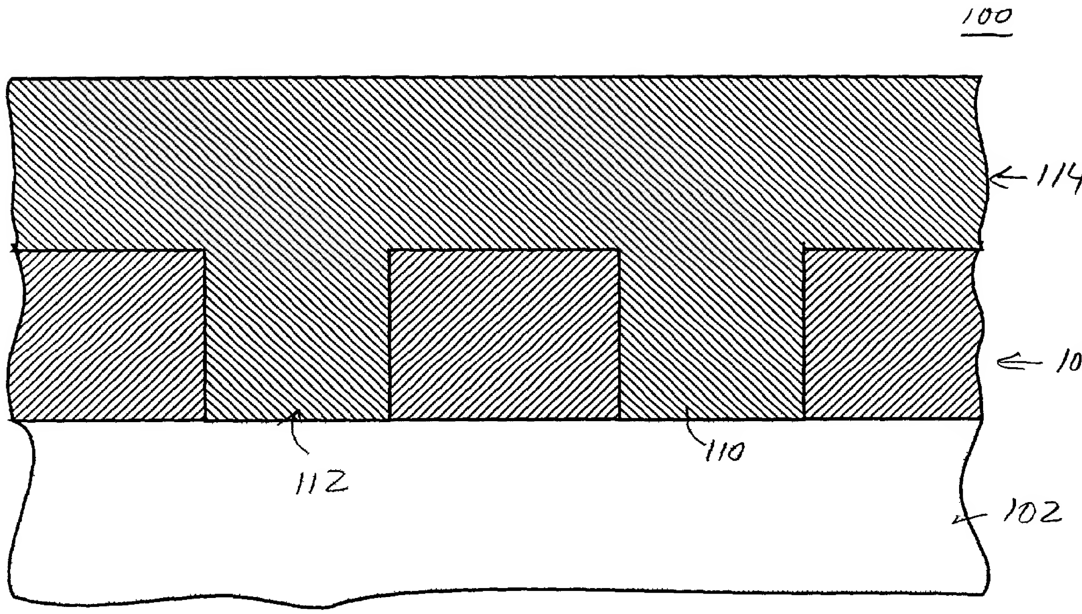

FIGURE 2C

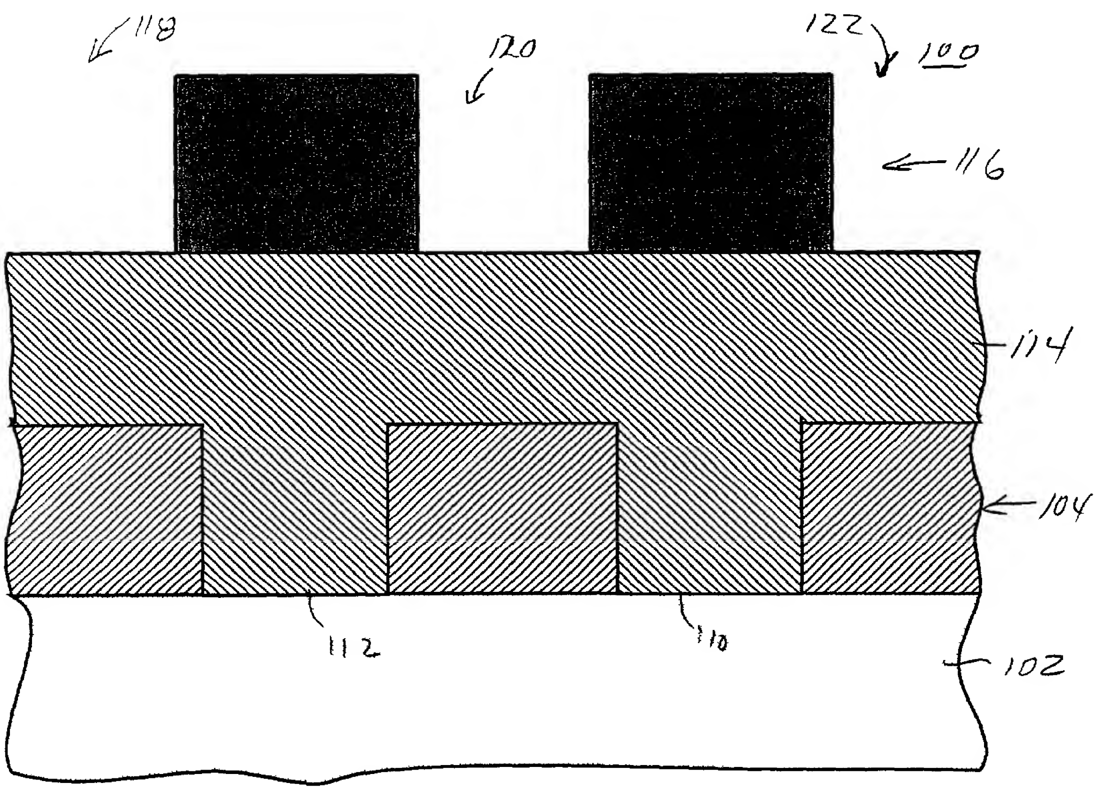

FIGURE 2D

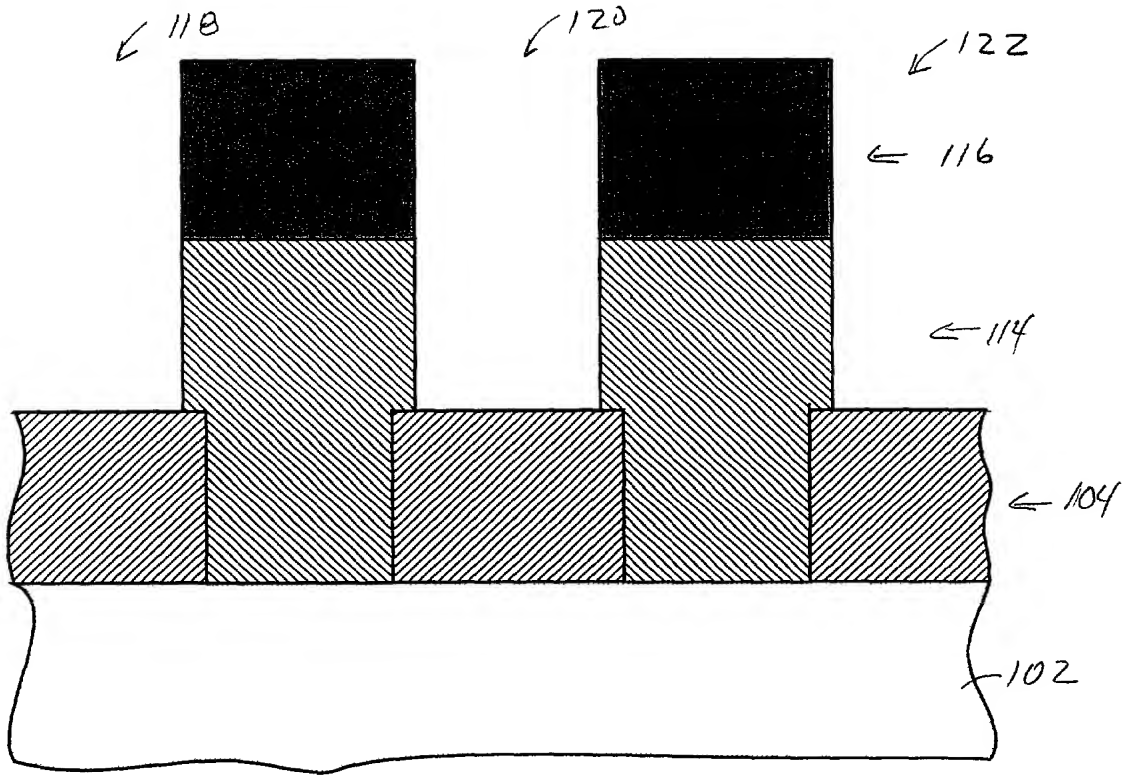

FIGURE 2E

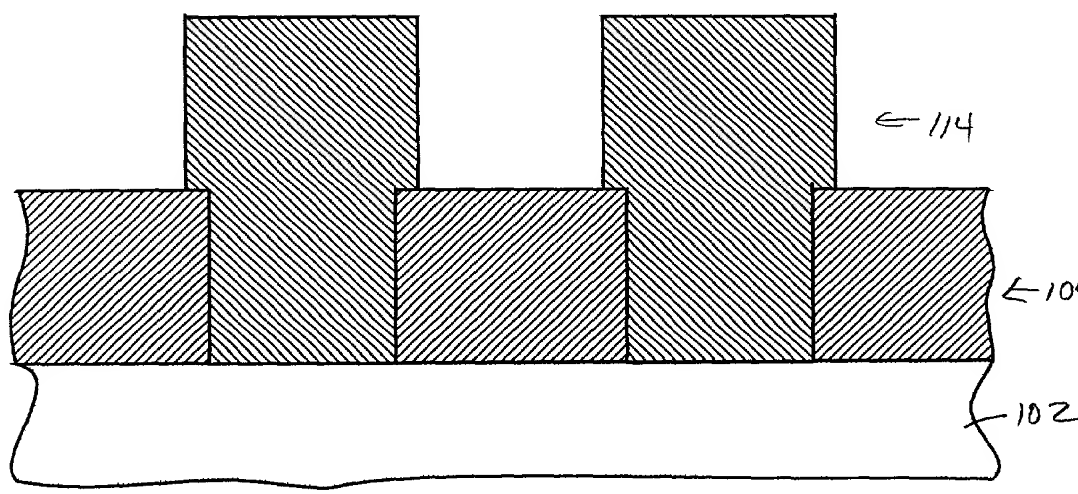

FIGURE 2F

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Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A SACRIFICIAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on ______________ as United States Application No. or PCT International Application Number ______________ and was amended on ______________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.) (Filing Date)

(Application Serial No.) (Filing Date)

(Application Serial No.) (Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

J. Vincent Tortolano, Reg. No. 31,433
Vincenzo D. Pitruzzella, Reg. No. 28,656
Richard J. Roddy, Reg. No. 27,688
William D. Zahrt II, Reg. No. 26,070
Louise K. Miller, Reg. No. 36,609
Paul S. Drake, Reg. No. 33,491
Louis A. Riley, Reg. No. 39,617
Rita M. Wisor, Reg. No. 41,382
Elizabeth A. Apperley, Reg. No. 36,428
H. Donald Nelson, Reg. No. 28,980

Send Correspondence to: **Law Office of H. Donald Nelson**
5492 Livorno Court
San Jose, CA 95138

Direct Telephone Calls to: *(name and telephone number)*
Don Nelson 408 239 0225

Full name of sole or first inventor	
Jeffrey A. Shields	
Sole or first inventor's signature: Jeffrey A. Shields	Date: 12/3/98
Residence: **Sunnyvale, California**	
Citizenship: **USA**	
Post Office Address: **445 Kenmore Avenue**	
Sunnyvale, CA 94086	

Full name of second inventor, if any	
Kelwin Ko	
Second inventor's signature	Date: 12/8/98
Residence: **San Jose, California**	
Citizenship: ~~USA~~ Hong Kong	
Post Office Address: ~~1130 Homer Common~~ 1717 Fumia Ct.	
San Jose, CA 95131	